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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/612,033	07/03/2003	Tadashi Iguchi	03180.0326	5852

7590 02/09/2005

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EXAMINER	
QUINTO, KEVIN V	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 02/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/612,033	IGUCHI ET AL.	
	Examiner	Art Unit	
	Kevin Quinto	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5 and 7-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *4,9-11,14,16,18 and 19* is/are allowed.

6)☒ Claim(s) *1,2,5,7,8,12,15,17 and 20* is/are rejected.

7)☒ Claim(s) *3 and 13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1, 2, 5, 12, 15, 17, and 20 have been considered but are moot in view of the new ground(s) of rejection.

2. The examiner notes newly amended claims 7 and 8. However the changes to these claims have lead to a new grounds for rejection (see below section titled *Claim Rejections - 35 USC § 112*).

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 7 and 8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5. With regard to claim 7, the applicant states "said word line is buried in said second trenches via a gate insulating film" in the last two lines. The preposition "via" does not appear to properly describe the applicant's actual structure since the word line is not buried in the second trench by way of the gate insulating film. Therefore the metes and bounds of claims 7 and 8 are rendered indefinite.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1, 2, 5, 12, 15, 17, and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Moriyama et al. (JP 2002-083884).

8. In reference to claims 1 and 12, Moriyama et al. (JP 2002-083884) discloses a similar device. Figures 12-22 disclose a non-volatile semiconductor memory device arranged in a matrix on a semiconductor substrate (1). Each cell in the matrix has a floating gate or electrode (104b). There are element isolating regions (110); each of which has a first trench, filled with an isolating filler, that is formed in the semiconductor substrate and between the memory cells adjacent each other along a gate width direction. There is a second trench formed in the isolating filler between the floating gates (104b) of the memory cells adjacent to each other along the gate width direction. The second trench has a narrower width at the bottom than at the top. The second trench has a maximum width that is smaller than the first trenches. A word line (114), buried in the second trenches, is connected to the memory cells and extends along the gate width direction. The fabrication process of the Moriyama device illustrated in figure 22 inherently meets claim 12.

9. In reference to claim 2, Moriyama meets the limitation of the claim. The applicant has disclosed that the parasitic capacitance can be reduced if the

second trench is shallower than the first trench (p. 9, lines 17-21 of applicant's specification). The Moriyama device illustrated in figures 12-22 meets this specified feature.

10. In reference to claims 5 and 15, Moriyama (JP 2002-083884) discloses a similar device. Figures 12-22 disclose a non-volatile semiconductor memory device arranged in a matrix on a semiconductor substrate (1). Each cell in the matrix has a floating gate or electrode (104b). There are element isolating regions (110); each of which has a first trench, filled with an isolating filler, that is formed in the semiconductor substrate and between the memory cells adjacent each other along a gate width direction. There is a second trench, in the shape of a U, formed in the isolating filler between the floating gates (104b) of the memory cells adjacent to each other along the gate width direction. The second trench has a maximum width that is smaller than the first trenches. A word line (114), buried in the second trenches, is connected to the memory cells and extends along the gate width direction. The fabrication process of the Moriyama device illustrated in figures 12-22 inherently meets claim 15.

11. In reference to claim 17, Moriyama (JP 2002-083884) discloses a similar device. Figures 12-22 disclose a fabrication process for a non-volatile semiconductor memory device arranged in a matrix on a semiconductor substrate (1). Each cell in the matrix has a floating gate or electrode (104b) with a predetermined gate width. A plurality of first trenches is formed (110) between adjacent floating gate electrodes (104b) along a gate width direction. The first trenches are self-aligned to the floating gate electrodes (104b). Element isolating

regions (110) are formed by filling isolating fillers in the first trenches. A sidewall spacer (111b) is on the surface of each of the isolating fillers (110) in a sidewall of the floating gate electrodes (104b). The sidewall spacer (111b) is in self-alignment with the floating gate electrodes (104b). A plurality of second trenches is formed in the isolating fillers (110) by using the sidewall spacers (111b) as a mask. The second trench has a narrower width at the bottom than at the top. The second trench has a maximum width that is smaller than the first trenches. A word line (114) is formed and is buried in the second trenches. The word line (114) extends along the gate width direction.

12. In reference to claim 20, each of the second trenches has a second gate insulating film (113) on its inner surface.

Allowable Subject Matter

13. Claims 4, 9, 10, 11, 14, 16, 18, and 19 are allowed.

14. Claim 3 and 13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

15. The following is a statement of reasons for the indication of allowable subject matter: the examiner is unaware of any prior art which suggests a semiconductor non-volatile memory device with a floating gate embedded within a trench formed within the trench insulation structures which isolate each memory cell where the trench has the shape of a V or an inverted trapezoid.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Quinto whose telephone number is (571) 272-1920. The examiner can normally be reached on M-F 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KVQ

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